AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph on page 1, lines 4-6 with the following amended paragraph:

This application claims the benefit of U.S. Provisional Application No. 60/282,723, filed April 9, 2001 (now abandoned), and U.S. Provisional Application No. 60/282,790, filed April 9, 2001 (now abandoned), both of which are hereby incorporated by reference.

Please replace the paragraph on page 2, lines 18-19 with the following amended paragraph:

Figure 1 is an illustration of a prior art page of memory ~~of a preferred embodiment~~ in accordance with a model set forth in the SmartMedia™ specification.

Please add the following new paragraphs following the last paragraph on page 2:

Figure 6 is a flowchart of a method for re-writing to a logical address of a write-once memory device of a preferred embodiment.

Figure 7 is a flowchart of a method for storing a file system structure in a write-once memory device of a preferred embodiment.

Figure 8 is a flowchart of a method for re-writing to a logical address of a write-once memory device of a preferred embodiment.

Figure 9 is a flowchart of a method for re-writing to a logical address of a write-once memory device of a preferred embodiment.

Figure 10 is a flowchart of a method for re-writing to a logical address of a write-once memory device of a preferred embodiment.

Please replace the paragraph on page 8, lines 1-17 with the following amended paragraph:

In the preferred embodiments described above, the data associating an individual physical address with an individual logical address was stored in a redundant field of a memory location. In an alternate embodiment, this data is stored in a separate table in the memory device. Analogous to a FAT table, as changes are made, data in this table can be updated to point to new areas. This table can be organized as a physical-to-logical table or a logical-to-physical table. Invalidating an entry in the table as bad can be done by any suitable method. For example, the entry can be "obliterated" overwriting at least a portion of the stored data with a destructive pattern, as described in U.S. Patent Application Serial No. 09/638,439 (now U.S. Patent No. 6,658,438), which is assigned to the assignee of the present invention and is hereby incorporated by reference. Additionally, a temporal-to-spatial mapping technique can be used to find the most-recent entry to the table. In this way, the act of storing new data invalidates the old data. The temporal-to-spatial mapping technique is described in U.S. Patent Application Serial No. 09/748,589 (pending), which is also assigned to the assignee of the present application and hereby incorporated by reference. Additionally, an invalid flag can be stored for the data associating a physical address with a logical address to invalidate that data. As used herein, the term "invalid flag" refers to one or more bits that are recognized as invalidating data that is associated with the flag.

Please replace the paragraph on page 10, line 16 – page 11, line 5 with the following amended paragraph:

The memory device can take any suitable form, such as a solid-state memory device (*i.e.*, a memory device that responds to electrical read and write signals to cause digital information to be read from and stored in a memory array of the device), a magnetic storage device (such as a hard drive), or an optical storage device (such as a CD or DVD). A memory device can comprise memory cells organized in a two-dimensional or three-dimensional array. In one preferred embodiment, the memory device takes the form of a solid-state memory device having a three-dimensional array of non-volatile write-once memory cells, as described in U.S. Patent No. 6,034,882 to Johnson et al., U.S. Patent No. 5,835,396 to Zhang, and U.S. patent application serial no. 09/560,626 (now abandoned), all of which are hereby incorporated by reference. As discussed in those documents, three-dimensional memory arrays provide important economies in terms of reduced size and associated reductions in manufacturing cost. Although any suitable type of memory cell can be used, in one preferred embodiment, the memory cell comprises an anti-fuse and a diode. The memory array can be made from any suitable material. In one preferred embodiment, the memory array comprises a semiconductor material. Other materials can be used, such as, but not limited to, phase-change materials and amorphous solids as well as those used with MRAM and organic passive element arrays, as described in U.S. Patent No. 6,055,180, which is hereby incorporated by reference. It is important to note that the following claims should not be read as requiring a specific type of memory array (*e.g.*, two-dimensional or three-dimensional) or material unless explicitly recited therein.

Please add the following new paragraphs between the paragraph on page 11, lines 6-13 and the paragraph on page 11, lines 14-21:

Turning again to the drawings, Figure 6 is a flowchart of a method for re-writing to a logical address of a write-once memory device. This method comprises the following: provide a write-once memory device, wherein the memory device stores first data in a memory location identified by a first physical address and further stores data that associates the first physical address with a first logical address (100), create a physical-to-logical address map from data stored in the memory device that associates physical addresses with logical addresses (110), store the second data in a memory location identified by a second physical address (120), invalidate the data stored in the memory device that associates the first physical address with the first logical address (130), and store data in the memory device associating the second physical address with the first logical address (140).

Figure 7 is a flowchart of a method for storing a file system structure in a write-once memory device. This method comprises the following: provide a write-once memory device comprising a plurality of blocks, each block comprising a data storing area, a first redundant field, and a second redundant field; wherein a block identified by a first physical address stores a file system structure in its data storing area and a first logical address in its first redundant field (150), create a physical-to-logical address map from data stored in the first and second redundant fields (160), from the physical-to-logical address map, determine that the first physical address is associated with the first logical address (170), write an invalid flag in a second redundant field of the block identified by the first physical address (180), write an updated file system structure in a data storing area of a block identified by a second physical address (190), and write the first

logical address in a first redundant field of the block identified by the second physical address (200).

Figure 8 is a flowchart of a method for re-writing to a logical address of a write-once memory device. This method comprises the following: provide a write-once memory device, wherein the memory device stores first data in a memory location identified by said logical address and further stores map data that associates a first physical address with a first logical address (210), store the second data in a memory location identified by a second physical address (220), and store second map data in the memory device associating the second physical address with the first logical address (230).

Figure 9 is a flowchart of a method for re-writing to a logical address of a write-once memory device. This method comprises the following: provide a write-once memory device, wherein the memory device stores first data in a memory location identified by said logical address and further stores map data that associates a first physical address with a first logical address, and further stores a used indicator flag associated with that first physical address (240), store the second data in a memory location identified by a second physical address (250), and store second map data in the memory device associating the second physical address with the first logical address (260).

Figure 10 is a flowchart of a method for re-writing to a logical address of a write-once memory device. This method comprises the following: provide a write-once memory device, wherein the memory device stores first data in a memory location identified by said logical address and further stores map data that associates a first physical address with a first logical address (270), perform a write at the logical address (280), read the data at the logical address to confirm the write succeeded or failed (290), store the second data in a memory location identified

by a second physical address only if the reading indicated a fail (300), and store second map data in the memory device associating the second physical address with the first logical address only if the reading indicated a fail (310).